1.1 Structure and Function of the Processor: 30-minute Pack

Total Marks

OCR H446 · Calculators not allowed · about 30 minutes

Name: _____ Date: ____ / ____ / _____

Answer ALL questions. Show all your working.

1 The Control Unit, Arithmetic Logic Unit and system clock each have a distinct role within the processor.

(a) State the purpose of the Control Unit (CU). **(2)**

(b) State the purpose of the Arithmetic Logic Unit (ALU). **(2)**

(c) State the purpose of the system clock in a processor. **(2)**

(Total for Question 1 is 6 marks)

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2 The processor uses several special purpose registers during the fetch, decode, execute cycle: the Program Counter (PC), Memory Address Register (MAR), Memory Data Register (MDR), Current Instruction Register (CIR) and the Accumulator (ACC).

(a) Complete the table by writing the correct register (PC, MAR, MDR or CIR) next to the function it performs. **(4)**

i) Holds the address of the next instruction to be fetched.

ii) Holds the address currently being accessed in memory, for a read or a write.

iii) Holds data or an instruction that has just been fetched from memory, or is about to be written to memory.

iv) Holds the instruction that is currently being decoded or executed.

(b) State the name of the register that holds the results of calculations performed by the ALU. **(1)**

(c) Explain why the Program Counter must be incremented during the fetch stage, even before the fetched instruction has been decoded. **(3)**

(Total for Question 2 is 8 marks)

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3 A processor has a clock speed of 3.2 GHz. On average, each instruction requires 4 clock cycles to complete.

(a) Calculate the number of instructions the processor can execute in one second. Show your working. **(3)**

(b) Explain why simply increasing clock speed indefinitely is not a practical way of improving a processor's performance. **(3)**

(Total for Question 3 is 6 marks)

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4 Cache memory is used to reduce the average time the processor spends waiting for data from RAM.

(a) State what is meant by 'cache memory'. **(2)**

(b) The principle of locality of reference underpins how cache improves performance. Describe what is meant by temporal locality and spatial locality, and briefly explain how each helps cache improve performance. **(4)**

(Total for Question 4 is 6 marks)

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Mark scheme · 1.1 Structure and Function of the Processor: 30-minute Pack

Question 1

(a) decodes the instruction held in the CIR oe **B1**

(a) generates and sends the control signals needed to coordinate/manage the components of the CPU during execution oe **B1**

(a) Answer: The CU decodes instructions and generates the control signals that coordinate the CPU's components.

(b) carries out arithmetic operations, e.g. addition, subtraction oe **B1**

(b) carries out logical operations/comparisons, e.g. AND, OR, NOT, greater than oe **B1**

(b) Answer: The ALU performs arithmetic operations (e.g. addition) and logical operations/comparisons.

(c) generates regular electrical pulses/a timing signal oe **B1**

(c) used to synchronise the operations of the CPU's components, controlling the rate at which instructions are processed oe **B1**

(c) Answer: The clock produces regular timing pulses that synchronise the CPU's components and set the rate of processing.

Question 2

(a) i) PC (Program Counter) **B1**

(a) ii) MAR (Memory Address Register) **B1**

(a) iii) MDR (Memory Data Register) **B1**

(a) iv) CIR (Current Instruction Register) **B1**

(a) Answer: i) PC, ii) MAR, iii) MDR, iv) CIR

(b) Accumulator (ACC) **B1**

(b) Answer: Accumulator (ACC)

(c) the PC must hold the address of the next instruction to be fetched oe **B1**

(c) incrementing it early ensures instructions are normally executed in the correct sequential order, one after another oe **B1**

(c) unless the current instruction is a jump/branch instruction, in which case the PC is overwritten with a new address once that instruction is executed oe **B1**

(c) Answer: The PC is incremented early so it is ready to point to the next sequential instruction, unless a jump/branch later overwrites it.

Question 3

(a) 3.2 GHz converted to Hz, i.e. 3.2 x 10^9 cycles per second, oe **M1**

(a) 3.2 x 10^9 divided by 4, correct method to find instructions per second oe **M1**

(a) 8 x 10^8 instructions per second, awrt (accept 800,000,000 or 800 million), cao **A1**

(a) Answer: 8 x 10^8 instructions per second (800,000,000)

(b) a higher clock speed causes the processor to generate more heat, which risks damage or errors if not adequately cooled oe **B1**

(b) a higher clock speed increases power consumption, which is a particular problem for battery powered/mobile devices oe **B1**

(b) there are physical limits to how fast transistors can reliably switch, and overall performance may also be limited by other bottlenecks (e.g. RAM speed), so gains are limited oe **B1**

(b) Answer: Higher clock speeds increase heat and power consumption and are limited by physical switching speed and other system bottlenecks, so performance gains are not unlimited.

Question 4

(a) a small amount of very fast memory, located on or very close to the CPU oe **B1**

(a) used to store instructions and data that have recently been used, or are likely to be needed again soon, to reduce the time spent accessing slower RAM oe **B1**

(a) Answer: Cache is a small, very fast memory close to the CPU that stores frequently/recently used instructions and data, reducing waiting time for RAM.

(b) temporal locality: if a memory location/instruction has recently been accessed, it is likely to be accessed again soon oe **B1**

(b) so keeping recently used items in cache means future requests for them can be served quickly from cache rather than slower RAM oe **B1**

(b) spatial locality: if a memory location is accessed, nearby/neighbouring locations are also likely to be accessed soon oe **B1**

(b) so when data is fetched, nearby memory locations are also copied into cache, meaning they will already be present when needed oe **B1**

(b) Answer: Temporal locality: recently used items are likely to be reused soon, so cache keeps them ready. Spatial locality: nearby locations are likely to be used soon, so cache pre-loads them too.

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