1.1 Structure and Function of the Processor: Test Pack

Total Marks

OCR H446 · Calculators not allowed · about 20 minutes

Name: _____ Date: ____ / ____ / _____

Answer ALL questions. Show all your working.

1 The Von Neumann model is the basis for most modern general purpose computer architectures.

(a) Define what is meant by the 'stored program concept'. **(2)**

(b) State the name of the CPU component that decodes fetched instructions, and the name of the component that carries out arithmetic and logic operations. **(2)**

(Total for Question 1 is 4 marks)

2 The width of the address bus determines the maximum amount of memory a processor can directly address.

(a) A processor has a 16-bit address bus. Calculate the maximum number of individually addressable memory locations this allows. Show your working. **(2)**

(b) The processor is replaced with a version that has a 32-bit address bus instead. Calculate how many times larger the maximum addressable memory becomes. **(2)**

(c) State one other factor, besides the width of the address bus, that can limit the amount of RAM a computer actually uses. **(1)**

(Total for Question 2 is 5 marks)

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3 Von Neumann and Harvard architectures organise memory and buses differently.

(a) Complete the table to compare Von Neumann and Harvard architectures. **(4)**

i) Von Neumann - memory arrangement:

ii) Von Neumann - bus arrangement:

iii) Harvard - memory arrangement:

iv) Harvard - bus arrangement:

(b) A manufacturer is designing the embedded processor for a domestic washing machine controller. Justify, with reference to the architectures compared in part (a), whether a Von Neumann or a Harvard architecture would be more suitable. **(4)**

(Total for Question 3 is 8 marks)

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Mark scheme · 1.1 Structure and Function of the Processor: Test Pack

Question 1

(a) program instructions and the data they operate on are held together, as binary values, in the same main memory oe **B1**

(a) instructions are fetched from memory and executed one at a time, in sequence, by the processor oe **B1**

(a) Answer: Instructions and data are stored together, as binary, in the same main memory, and instructions are fetched and executed one at a time in sequence.

(b) Control Unit (CU) **B1**

(b) Arithmetic Logic Unit (ALU) **B1**

(b) Answer: Control Unit (decodes instructions); Arithmetic Logic Unit (arithmetic and logic operations).

Question 2

(a) 2^{16} shown as the method oe **M1**

(a) 65536, cao **A1**

(a) Answer: 65536 memory locations

(b) 2^{32} divided by 2^{16} (or 2^{32-16}) shown as the method oe **M1**

(b) 65536 times larger, cao (accept 2^{16}) **A1**

(b) Answer: 65536 times larger

(c) any one of: limitations of the operating system (e.g. a 32-bit OS may only support up to 4GB); the amount of RAM physically installed/available on the motherboard; cost oe **B1**

(c) Answer: For example, the operating system's own addressing limit, or the amount of RAM physically installed.

Question 3

(a) i) instructions and data are stored together in a single, shared main memory oe **B1**

(a) ii) a single, shared bus system connects the CPU to memory, so an instruction and a data value cannot be transferred at exactly the same time oe **B1**

(a) iii) instructions and data are stored in separate, independent memories oe **B1**

(a) iv) separate bus systems connect the CPU to each memory, allowing an instruction and a data value to be transferred at the same time oe **B1**

(a) Answer: Von Neumann: shared memory, shared bus. Harvard: separate memories, separate buses (allowing simultaneous access).

(b) **L2** A clear, justified conclusion (Harvard or, if soundly reasoned, Von Neumann) that correctly applies at least two relevant features of the architectures (e.g. simultaneous instruction/data access, real-time response, program size/fixed function, cost, flexibility) to the specific context of an embedded washing machine controller. Correct terminology is used. **3-4**

(b) **L1** A basic or partial answer, e.g. states which architecture is used in embedded systems generally, or identifies one relevant feature, without clearly applying it to the washing machine scenario. **1-2**

(b) **L0** No relevant content, or the response does not address the scenario. **0**

(b) Indicative content:

- A washing machine controller runs a small, fixed, dedicated program that must respond to sensors (e.g. water level, door lock) in real time
- Harvard architecture allows an instruction and a data value to be fetched/accessed at the same time, giving faster, more predictable execution, which suits real-time control
- This can make the controller more reliable/responsive, which is important for safety-critical actions such as controlling the heater or door lock
- A counter-argument: Von Neumann architecture is simpler and cheaper to implement, and for a program this small the shared-bus bottleneck may have little practical effect
- Either conclusion (Harvard or Von Neumann) can be credited if it is clearly justified using relevant, accurately applied points about the two architectures
- Accept a balanced answer that weighs speed/reliability (favouring Harvard) against simplicity/cost (favouring Von Neumann)

(b) Answer: Harvard architecture is generally more suitable, since simultaneous instruction/data access gives faster, more predictable real-time response for safety-relevant control; a well-justified case for Von Neumann on cost/simplicity grounds can also be credited.

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