1.6 Computer Architecture, Assembly and the LMC: 10-minute Pack

OCR H446 · Calculators not allowed · about 10 minutes

Total Marks

Name: _____ Date: ____ / ____ / _____

Answer ALL questions. Show all your working.

1 Two assembly instructions are STA 250 (store the value in the accumulator directly to memory address 250) and BRA 50 (branch always to the instruction at address 50).

(a) Using register transfer notation, describe the execute stage of STA 250. **(3)**

(b) Using register transfer notation, describe the execute stage of BRA 50. **(2)**

(c) Explain how the execute stage of BRA 50 is able to change the normal sequential order in which instructions are fetched. **(2)**

(Total for Question 1 is 7 marks)

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Mark scheme · 1.6 Computer Architecture, Assembly and the LMC: 10-minute Pack

Question 1

(a) MAR <- 250, oe (the operand address is copied to the MAR) **M1**

(a) MDR <- [ACC], oe (the value to be written is copied from the accumulator to the MDR) **M1**

(a) [[MAR]] <- [MDR], oe (the value in the MDR is written to the memory location addressed by the MAR) **A1**

(a) Answer: MAR <- 250; MDR <- [ACC]; [[MAR]] <- [MDR]

(b) PC <- 50, oe (the operand value from the CIR is copied directly into the PC) **M1**

(b) correctly identifies that no memory read or write, and no change to the ACC, is needed to carry this out **A1**

(b) Answer: PC <- 50

(c) normally the PC is incremented by 1 during fetch so that it points to the next instruction in sequence oe **B1**

(c) the execute stage of BRA overwrites the PC with the operand address instead, so the next fetch reads the instruction at that new address rather than the following one oe **B1**

(c) Answer: Because the execute stage of BRA directly overwrites the PC with a new address, the next fetch reads from that address instead of the next sequential one.

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