1.1 Systems Architecture: Test Pack

OCR J277 · Calculators not allowed · about 20 minutes

Total Marks

Name: _____ Date: ____ / ____ / _____

Answer ALL questions. Show all your working.

1 Which of these best describes the purpose of the CPU?

(a) Identify the correct description of the purpose of the CPU. **(1)**

- ☐ A) To store data permanently when the computer is switched off
- ☐ B) To fetch, decode and execute instructions
- ☐ C) To provide long term storage for the operating system
- ☐ D) To convert analogue signals into digital signals

(Total for Question 1 is 1 mark)

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2 Not all computer systems are general purpose computers. Some are embedded systems.

(a) Define the term 'embedded system' and give two examples of a device that contains one. **(3)**

(Total for Question 2 is 3 marks)

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3 The von Neumann architecture uses buses to transfer information between the CPU and memory.

(a) State the purpose of the address bus. **(1)**

(b) State the purpose of the data bus. **(1)**

(c) State the purpose of the control bus. **(1)**

(Total for Question 3 is 3 marks)

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4 CPUs contain a small amount of cache memory.

(a) Explain what cache memory is and explain how it can improve CPU performance. **(3)**

(Total for Question 4 is 3 marks)

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5 Describe how the fetch, decode, execute cycle uses registers to process an instruction.

(a) Describe the fetch, decode, execute cycle, referring to the registers involved. **(4)**

(Total for Question 5 is 4 marks)

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6 A CPU has an address bus that is 16 bits wide.

(a) Calculate the maximum number of individually addressable memory locations this allows. Show your working. **(2)**

(Total for Question 6 is 2 marks)

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Mark scheme · 1.1 Systems Architecture: Test Pack

Question 1

(a) B, fetch, decode and execute instructions **B1**

(a) Answer: B

Question 2

(a) a computer system built into a larger device or product to perform a specific, dedicated function, oe **B1**

(a) example 1, e.g. washing machine, microwave, digital thermostat, traffic light controller, car engine management system (any suitable device) **B1**

(a) example 2, a different suitable example to the one already given **B1**

(a) Answer: A computer system built into a device to perform a specific task, e.g. washing machine, digital thermostat.

Question 3

(a) carries the memory address of the location to be read from or written to, oe **B1**

(a) Answer: Carries the address of the memory location being accessed.

(b) carries the actual data or instructions being transferred between the CPU and memory, oe **B1**

(b) Answer: Carries the data/instructions being transferred between CPU and memory.

(c) carries control signals (e.g. read/write signals) that coordinate and synchronise the transfer of data between components, oe **B1**

(c) Answer: Carries control signals that coordinate data transfer between the CPU and memory.

Question 4

(a) cache is a small amount of very fast memory located on, or very close to, the CPU, oe **B1**

(a) it stores instructions and data that have recently been used or are likely to be needed again soon, oe **B1**

(a) so the CPU can access this data more quickly than fetching it from RAM each time, reducing waiting time and improving performance, oe **B1**

(a) Answer: Cache is small, fast memory close to the CPU that stores frequently/recently used data, reducing the need to access slower RAM.

Question 5

(a) One correct point about how the cycle uses the registers, from: the address in the PC is copied to the MAR; the instruction stored at that address is copied from memory to the MDR; the PC is incremented so it holds the address of the next instruction; the instruction in the MDR is copied to the CIR; the instruction in the CIR is decoded (by the control unit); the instruction is then executed and the cycle repeats **B1**

(a) A second, different correct point from the same list **B1**

(a) A third, different correct point from the same list **B1**

(a) A fourth, different correct point from the same list. Any four from the six points (max 4 marks awarded overall), accept points in any logical order; do not credit the same point twice **B1**

(a) Answer: PC to MAR, fetch from memory to MDR, PC incremented, MDR to CIR, decode, execute; repeat.

Question 6

(a) 2^{16} shown as the method, oe **M1**

(a) 65536, cao **A1**

(a) Answer: 65536 memory locations

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